Fabrication of a micro-cantilever gold plated beams array

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Abstract

Purpose – The processing techniques and materials utilized in the fabrication of a two-terminal electrostatically actuated micro-electro-mechanical cantilever-arrayed device used for radio frequency tuning applications are presented in this work. The paper aims to discuss these issues.

Design/methodology/approach – The process, which is based on silicon surface micromachining, uses spin-coated photoresist as the sacrificial layer underneath the electroplated gold structural material and an insulating layer of silicon dioxide, deposited using plasma enhanced chemical vapour deposition (PECVD), to avoid a short circuit between the cantilever and the bottom electrode in a total of six major fabrication steps. These included the PECVD of the silicon dioxide insulating layer, optical lithography to transfer photomask layer patterns, vacuum evaporation to deposit thin films of titanium (Ti) and gold (Au), electroplating of Au, the dry release of the cantilever beam arrays, and finally the wafer dicing to split the different micro devices. These process steps were each sub-detailed to give a total of 14 micro-fabrication processes.

Findings – Scanning electron microscope images taken on the final fabricated device that was dry released using oxygen plasma ashing to avoid stiction showed 12 freely suspended micro-cantilevered beams suspended with an average electrostatic gap of 2.29 $\pm$ 0.17 μm above a 4,934 $\pm$ 3 Å thick silicon dioxide layer. Preliminary dimensional measurements on the fabricated devices revealed that the cantilevers were at least 52.06 $\pm$ 1.93 μm wide with lengths varying from 377.97 $\pm$ 0.01 to 1,491.89 $\pm$ 0.01 μm and were at least 2.21 $\pm$ 0.05 μm thick.

Originality/value – The cantilever beams used in this work were manufactured using electroplated gold, and photoresist was used as a sacrificial layer underneath the beams. Plasma ashing was used to release the beams. The beams were anchored to a central electrode and each beam was designed with varying length.

Keywords Semiconductor technology, Chip scale packaging, Die/dicing technology, Micro electro mechanical systems, Microelectronics packaging, Thick/thin film technology

Paper type Research paper

Introduction

Micro-electro-mechanical systems (MEMS) or micromachines are an important innovation in technology that have recently shown dramatic advances in the semiconductor industry (Madou, 2002). This technology enables the fabrication of machines that are vanishingly small, very cheap, and have the ability to function in a variety of applications. However, to achieve these attributes, there is always need to optimize the MEMS fabrication process so that it involves less steps, uses fewer lithographic masks, and achieves a high yield. The process presented in this work uses three photomasks in a six step fabrication process, which includes a final dry release step aimed at achieving fully suspended stiction free MEMS-cantilevers thus increasing the yield. A sketch of the suspended MEMS-cantilever is shown in Figure 1 and fabricated devices in Figure 2. Micromachining, microfabrication, micromanufacturing and MEMS fabrication all relate to processes aimed at developing devices with at least some of their dimensions in the micrometer range, and whose applications extend from silicon-based mechanical purposes to biotechnology, and information and communication technologies (Petersen, 1982). As a result, MEMS refers to all sub-miniaturised systems including silicon-based mechanical devices, chemical and biological sensors and actuators, and miniature non-silicon structures (e.g. devices made from plastics or ceramics).

Overall, applications areas of MEMS are in miniaturized devices in the automotive industry used for physical sensing (Guckel, 1991) and actuation (Sniegowski and Garcia, 1996); miniature sensors and instruments in medical and biotechnology applications based on chemical sensing (Krebs, 1993); miniature devices in information technology (IT) and peripherals (including hard disk drive heads, micro-displays, and ink-jet print heads); optical steering in telecommunications and industrial automation (Smith *et al.*, 1996). Several fields and products have emerged over the years based on the applications of MEMS. BIOMEMS (which includes microfluidic structures, immunosensors, DNA arrays, etc.) deals with life-saving disposable diagnostic sensors, systems speeding up drug discovery (Shawgo *et al.*, 2002), small pills for improving delivery, etc. most of these devices being disposable (Li *et al.*, 2002a, b). Mechanical MEMS deals with micro-resonant sensors like accelerometers and gyroscopes. Optical MEMS or MOEMS involve micromirror arrays, fiber optic connectors, etc. whereas radio frequency MEMS (RFMEMS) involve inductors, capacitors, antennas, etc. (De Luis *et al.*, 2010). Commercial off-the-shelf microelectromechanical systems or COTS_MEMS (Holbert *et al.*, 2010), and high-aspect-ratio MEMS (HARMEMS) have also been introduced (Hutchison *et al.*, 2010), and many more are expected.

MEMS devices can be made cheap because they are prepared by exploiting the existing integrated circuit manufacturing

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Figure 1 Sketch of a suspended MEMS-cantilever

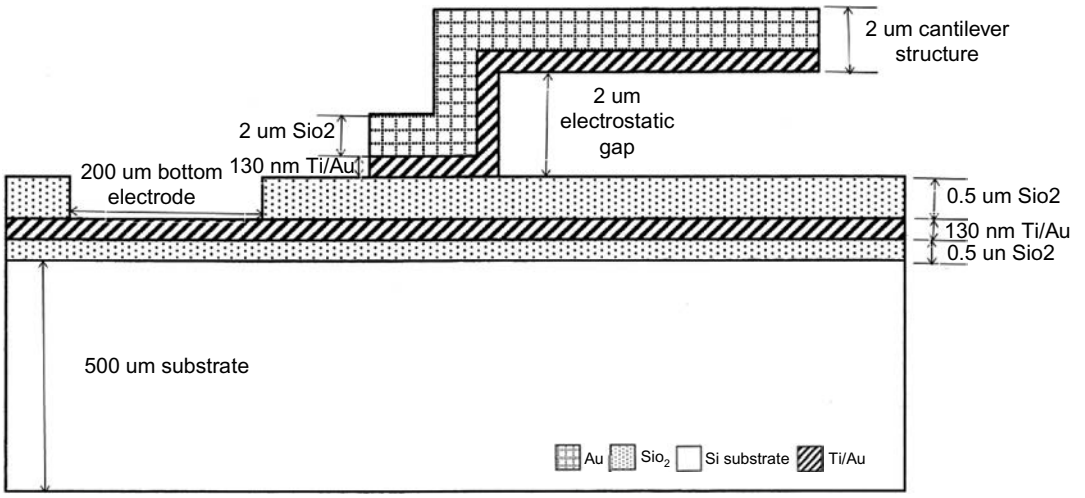
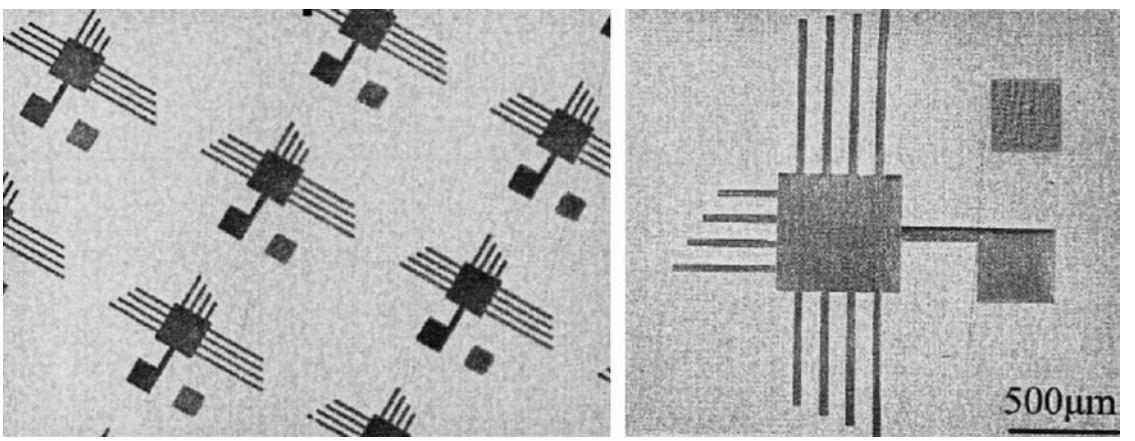


Figure 2 (a) SEM pictures of many fabricated devices on a single wafer before dicing; (b) close-up of a diced MEMS-cantilever device



(a) **(b)**

infrastructure (Smith *et al.*, 1995). Consequently, MEMS structures are created through successive deposition (Mattox, 2010), photo-patterning (Kao *et al.*, 2010), and then etching of thin films of silicon (Eidelloth, 1991), a process referred to as silicon micromachining (Jung *et al.*, 2010). Recently, nanomachining or nanoelectromechanical systems (NEMS) that extend micromachining in a typical top-down approach into the submicron range relying mostly on advanced semiconductor fabrication methods, have also been explored (Shida *et al.*, 2011). The quest for nanoscale architectures has also given impetus to bottom-up techniques with methods including self-assembly of metal, semiconductor and other particles, template chemistry and mechanosynthesis (Buffa *et al.*, 2012).

MEMS fabrication uses high volume semiconductor batch processing that involves the addition or subtraction of two dimensional layers on a substrate using photolithographic patterning as well as chemical etching. In general, the fabrication of MEMS devices falls in three general classifications: bulk micromachining (Ghaemi *et al.*, 2011); surface micromachining (Liu *et al.*, 2010); and high-aspect-ratio micromachining (HARM) that also includes the Lithographie Galvanoformung Abformung (LIGA) technique based on lithography, electroforming and moulding. In bulk micromachining structures are realized through the removal of part of the bulk substrate in a subtractive process to create pits, grooves and channels using dry or wet anisotropic etching methods, whereas in surface micromachining, processing is done above the substrate by mainly using it as a foundation layer to build on structures through successive thin film deposition and etching steps. HARM on the other hand involves micromachining as a tooling step followed by injection moulding or embossing, or even electroforming to replicate microstructures in metal from moulded parts (Li *et al.*, 2011).

In this work, surface micromachining was used on silicon (Si) substrates or wafers to fabricate MEMS structures in a class 1,000 clean room facility (Kim *et al.*, 2001). Phosphorous N-doped, single-side polished, 500 μm thick Si wafers were used for the work. The material used in fabricating the vibrating structures was gold (Au); chosen because of its good conductivity and reflective surfaces that eases optical resonance measurements (Villain *et al.*, 2008).

A thin layer of Au deposited on top of titanium (Ti) was also used to define the bottom actuating electrode (Winter, 1993-2012). There were six key processing techniques used in the fabrication. These were: plasma enhanced chemical vapour deposition (PECVD); optical lithography; vacuum evaporation (Klenk *et al.*, 1993); electroplating (Angurel *et al.*, 2007); dry release (Keller *et al.*, 2007); and wafer dicing (Lee *et al.*, 2007). The processing steps are shown in Figure 3, and explained below in more details.

PECVD was used for the deposition of 0.5 μm of silicon dioxide (SiO_2) insulating layer using the Surface Technology Systems (STS) PECVD tool (Roszairi and Rahman, 2002). In PECVD, a plasma is used to activate radicals, ions or highly excited species, which results in the deposited film whereas the ion bombardment of the substrate provides the energy required for them to settle as a stable film after interaction (Bhal Singh *et al.*, 2011). Although it results into chemical particle contamination in form of hydrogen ions, PECVD is widely used because of its low substrate temperature, good adhesion, low pinhole density, as well as good coverage (Reif and Kern, 1991). PECVD is shown by letters A and C in Figure 3(a).

Photolithography was used for optical patterning of the deposited layers before etching to form the required structures (Sun and Rusli, 2011). This process was composed of photoresist spin coating, soft baking of the coated wafer to promote photoresist adhesion and release of any solvent, photomask alignment followed by ultraviolet exposure, and finally the photoresist develop. A positive photoresist was used that meant that the exposed areas of the pattern were removed by the developer (Wong, 2001). Photolithography is shown by letters D, F and H in Figure 3(a).

Vacuum evaporation (Li *et al.*, 2002) was used for the deposition of the thin film layers of Ti and Au inside a BOC Edwards Auto 500 evaporator (Miranda *et al.*, 2010). It is a form of physical vapour deposition (PVD) inside a low pressure PVD reactor in which the vaporised materials encounter few intermolecular collisions while travelling to the substrate in a line of sight format (Yeganeh and Torabi, 2011). Vacuum evaporation is shown by letters B and G in Figure 3(a).

Electroplating was used for the electrodeposition of Au onto a dielectric silicon dioxide layer coated with a low resistance, thin adhesive film of Ti acting as a seed layer (Brenner, 1963). Areas for electrodeposition are normally defined by a ultraviolet (UV) exposed pattern in a spin-coated polymer, which on developing away the exposed resist, establish contact with the seed layer (Parthasaradhy, 1989). This process was carried out in an electrolytic cell with the surface to be plated acting as the cathode in a plating solution made of the metal to be deposited, and the anode made of a material not readily attacked by the solution. Electroplating is shown by letters I in Figure 3(a).

Dry release was used as a stiction-free oxygen plasma stripping or ashing process of the photoresist layer which was acting as a sacrificial layer, resulting into a free hanging structure (Han *et al.*, 2003). Unlike wet stripping, dry release is controllable, causes no photoresist undercuts or broadening, is less corrosive and leaves a cleaner surface (Shuzo *et al.*, 1991). Dry release is shown by letter L in Figure 3(a).

Wafer dicing is the sawing process of the finished wafer into the individual dies or devices ready for packaging and testing. With the wafer mounted on a sticky tape onto the dicing saw machine, a saw blade consisting of a thick-shaped hub a diamond or carbide grit impregnated rim and rotating at several thousand revolutions per minute, encounters the wafer at a feed rate of the order of a centimetre per second to partially or completely cut through it (Lee *et al.*, 2007).

Methodology

This fabrication process was intended to solve the design challenges and carefully arranged such that all steps are sequentially compatible to each other. The advantages of this fabrication process are its simplicity: the fact that it is released on the wafer level using surface micromachining as opposed to bulk micromachining; it employs only standard micromachining procedures like evaporation, photolithography, etc. and it uses only three masks. The process steps followed in the fabrication of the prototype for the testing frequency tuning are outlined in Figure 3(b). From this flow chart, the major steps are:

1 Deposition of initial SiO_2 insulation, lower (Ti/Au) metal electrode, the second SiO_2 insulation, and the sacrificial layer.
2 Vacuum evaporation of Ti/Au seed layer, electroplating of gold as the main structural material.
3 Release of the plated device. An illustration of the major steps is shown in Figure 3(a).

Wafer cleaning

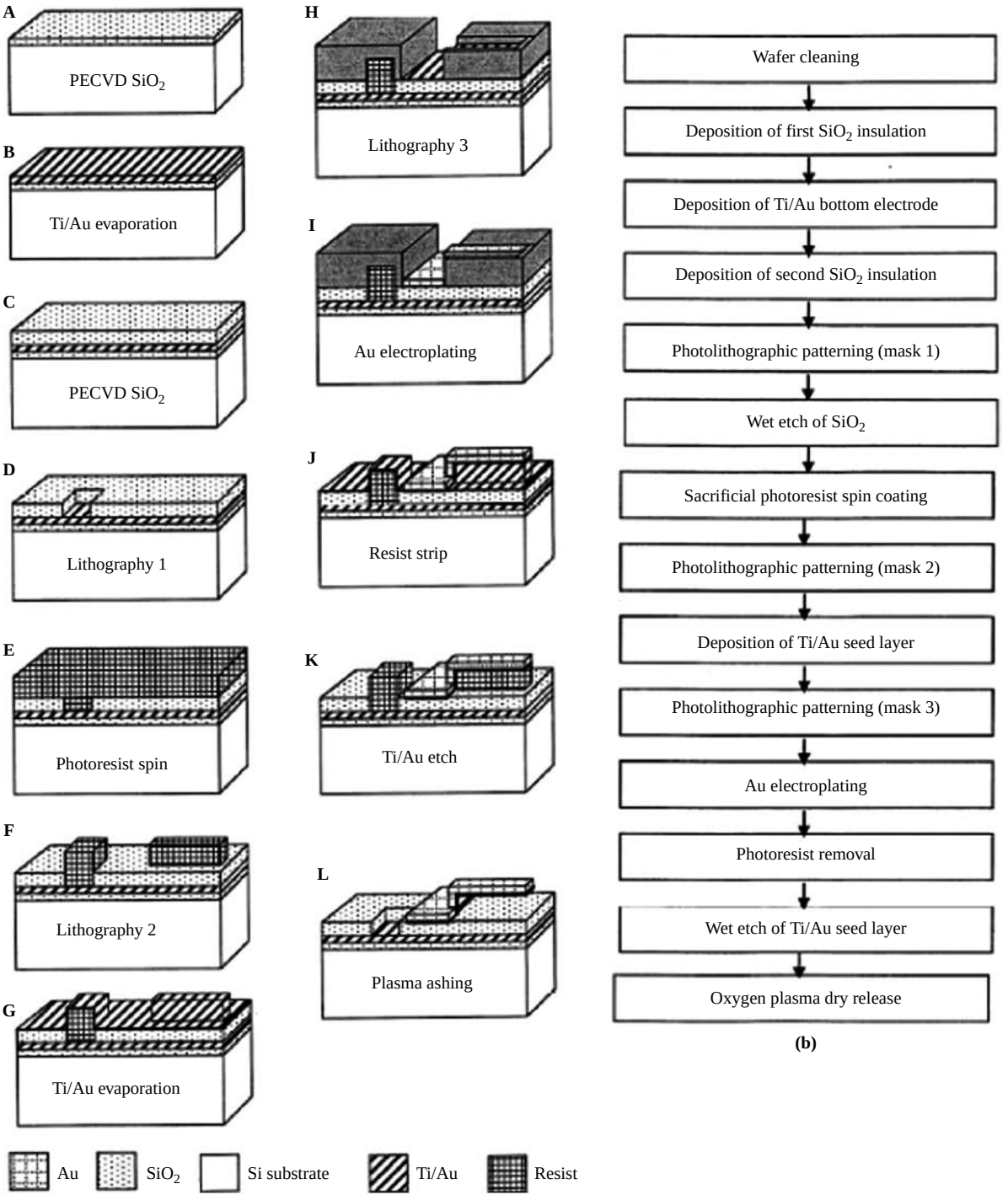
For high performance and high reliability microelectromechanical devices, and to prevent contamination of process equipment, contaminants present on the surfaces of silicon wafers need to be removed (Osaka and Hattori, 1998). Contaminants include solvent strains (methyl alcohol, acetone, trichloroethylene, isopropyl alcohol, xylene, etc.), dust from operators and equipment, smoke particles, etc. The industry standard Radio Corporation of America (RCA) is the wet cleaning method that uses a mixture of hydrogen peroxide (H_2O_2) and various acids or bases followed by deionized water (DI) rinses. A thin oxide layer is left after the RCA cleaning, and is removed by dipping the wafer in a 1 per cent aqueous hydrofluoric (HF) solution for short time. The RCA1 and RCA2 wet cleaning procedures followed in cleaning the wafers before any process was performed were as follows.

In RCA1 one part of 25 per cent aqueous ammonium solution (NH_3) was added to five parts of DI water, and heated to boil before adding one part of H_2O_2 Wafers were then immersed into the mixture for ten minutes. This cleaning procedure was used to remove organic deposits on the wafer including resist.

In RCA2, one part of hydrochloric acid (HCl) was added to six parts of DI water, and heated to boil before adding one part of H_2O_2 Wafers were then immersed into the mixture for ten minutes. This cleaning procedure was used to remove metal ions and is required to keep oxidation and diffusion furnaces free of metal contamination (Ouimet *et al.*, 1996).

After other wafer processes, piranha, which is a boiling solution of sulphuric acid and hydrogen peroxide, was employed to remove both organic and metallic contaminants. Use of any of the above solutions will remove the metal pattern on the substrate so this cleaning technique was avoided after the evaporation and electroplating steps. Under these circumstances, alternative cleaning methods were used. These included dipping the wafer in isopropyl alcohol (IPA), and then into acetone both of which helped to degrease the

Figure 3 (a) Simplified fabrication process; (b) outline of the fabrication process showing all the major steps

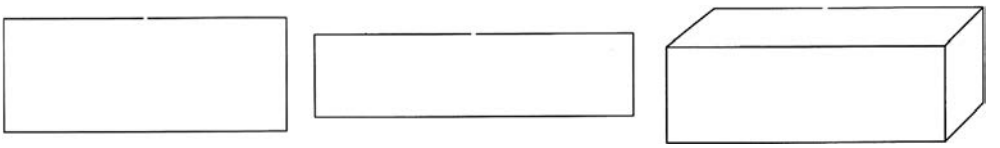


surface of the wafer and at the same time rinse off the surface particulate. The wafer was then dipped into a DI water bath with ultrasonic agitation to facilitate further cleaning. The final cleaning was then done in a rinse-drier where high spin speeds produced centrifugal forces that expelled more particles from the wafer surfaces (Kern, 1993). Figure 4 shows the sketch of the substrate after wafer cleaning (Figure 5).

Deposition of first insulating silicon dioxide layer

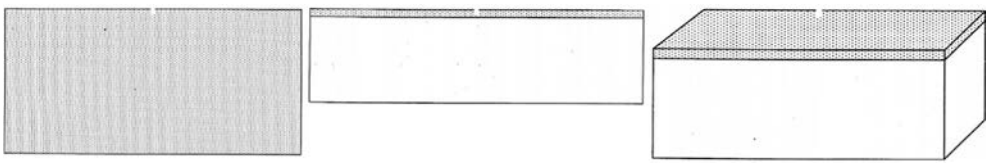
The fabrication of the two-terminal device began with 0.5 μm of PECVD SiO_2 onto the silicon wafer to insulate the Ti/Au from contact with the silicon substrate (Yee *et al.*, 2010). The thickness of the PECVD SiO_2 was measured using the Filmetrics F20 thin film measurement system. This instrument can be used to determine the thickness as well as optical constants (n and k) of

Figure 4 Silicon substrate after SC1 cleaning



Notes: (a) Top view; (b) side view; (c) 3-D view

Figure 5 PECVD SiO_2 of 0.5 μm nominal thickness



Notes: (a) Top view; (b) side view; (c) 3-D view

transparent and semi-transparent thin films. The measurement process involved placing the wafer below optical beam at different locations along the beam and monitoring the thicknesses. SiO_2 thicknesses were measured from five different locations around four wafers and the overall average thickness of the deposited PECVD oxide was 5,181 ± 26 Å.

The wafers were also analysed using the MTI Proforma 200S measurement system to determine the resultant wafer curvature or bow, and therefore the stress in the deposited oxide. From the measurements, it was noted that the bow increased following the oxide deposition, which signified an increase in the stress, although for the purposes of this work the oxide was used mainly for insulation between the silicon substrate and the bottom Ti/Au metal layer, and would not after device performance. The bow changed from 6.65 to 9.77 μm after the SiO_2 deposition.

Deposition of bottom Ti/Au metal electrode

In this work, the vacuum evaporation techniques was employed to deposit thin electrically conductive metal films forming the bottom actuation electrode used in the electrostatic pull-down process and resultant frequency tuning (Geng, 2005). Titanium (Ti) metal, 30 nm thick was evaporated onto the insulating SiO_2, followed by 100 nm of Gold (Au) as shown in Figure 6. Ti readily adheres to the surface of the oxide and to Au. Gold was chosen for its low resistivity, ease during both evaporation and wire bonding while packaging. The BOC Edwards Auto 500 evaporator (Edwards Limited, 2012) was used to deposit the Ti/Au lower metal electrode.

Deposition of second insulating SiO_2 layer

The second insulating layer of SiO_2 was deposited by plasma enhance chemical vapour deposition (PECVD). This layer was used to prevent a short circuit between the bottom Ti/Au metal electrode and the top electrode during electrostatic actuation. The sketch for this step is shown in Figure 7. The wafer curvature, thickness, and stress in the oxide were measured after the deposition showing a bow of 15.96 μm. The average thickness of the deposited silicon oxide insulating layer was 4,934 ± 3 Å.

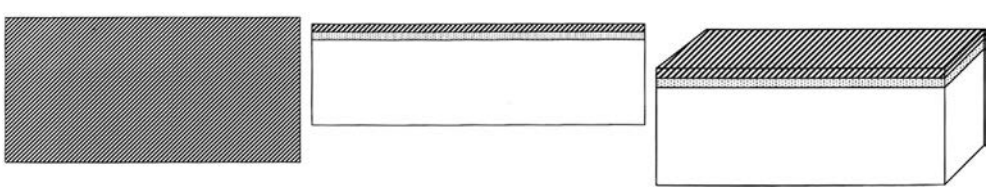
Photolithography defining the bottom electrodes

Photolithography was the technique used to transfer copies of a master pattern onto the surface of a wafer (Scheer *et al.*, 2010). Photolithography is the widely used form of lithography and was done following a set of process steps. In the first step of the lithography step, a thin layer of an organic polymer, a photoresist sensitive to ultraviolet radiation was spin coated onto the wafer. Prior to this, a resist adhesion promoter, hexamethyldisilazane (HMDS) was applied as a vapour in a YES 310 TAE oven in order to prepare the surface for the deposition of the photoresist (Ronghua, 2010).

A positive photoresist SPR700 of thickness 7 μm was dispensed from a viscous solution of the polymer onto the wafer held by a vacuum chuck lying on a wafer platen in a resist spinner using the EV101 spin-coater. The wafer was then spun at high speeds so that the generated centripetal force causes the solution flow to edges thus making a uniform film.

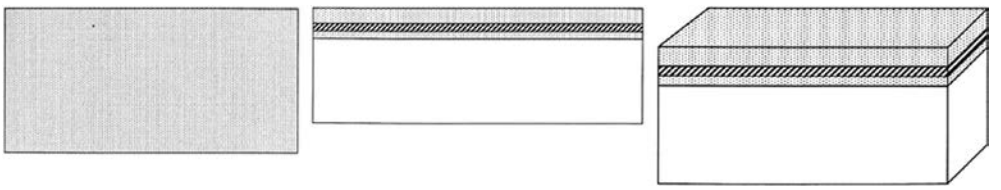
After spin coating, the wafers were soft baked at 90°C for three minutes to remove solvents and stresses, and to promote

Figure 6 Ti/Au evaporation of bottom electrode: 30 nm/100 nm thicknesses



Notes: (a) Top view; (b) side view; (c) 3-D view

Figure 7 PECVD SiO_2 of 0.5 μm thickness



(a) **(b)** **(c)**

Notes: (a) Top view; (b) side view; (c) 3-D view

adhesion of the resist layer to the wafer. Following the soft baking, transfer of the patterns on the lithographic mask M1 to the resist-coated wafer was performed using the EV620 contact aligner. The aligner performed the contact alignment of the wafer and the mask, and then exposed the wafer to ultraviolet (UV) light. A 7 μm recipe was used that allowed a UV exposure time of 18 s. The EV102 photoresist developer was then used to reveal the exposed patterns on the wafer. Figure 8 is the sketch showing the lithography step for the bottom electrode.

A mild oxygen plasma treatment, also called descumming, was used to remove unwanted resist left behind after development. Post baking or hard baking was then done to remove residual solvents. The baking process also anneals the film to promote interfacial adhesion of the resist that would have been weakened either by developer penetration along the resist/substrate interface or by swelling of the resist (mainly for negative resists). Hard baking also improves hardness of the film, which increases the resistance of the resist to subsequent etch steps. The heat application in hard baking can result in excessive resist flow and melt which degrades wall profile angle and makes it difficult to remove the resist.

Wet etching of the second oxide layer

A wet etch using buffered HF was then performed to remove the patterned SiO_2 so as to expose the lower contact pads, metallic lines, and dicing lines. Before the wet etching, a low-power oxygen (O_2) plasma ashing also called a descum, was done to remove all impurities from the areas to be etched. This was done using the Tepla 300 plasma asher with a plasma power setting of 250 w at an O_2 flow rate of 800 ml/min and chamber pressure of ~1mbar for 20 s. In this work, a 7:1 buffered hydrofluoric acid solution (BHF) at room temperature was used to etch the oxide layer using the photoresist as a mask to a target depth of 0.5 μm so as to expose the Ti/Au bottom electrode. The wet etching solutions comes factory set with HF and ammonium hydroxide (NH4OH) in a 7:1 ratio (Eidelloth, 1991). An etch rate of 3,400 Å/min at room temperature was used for the etching of the SiO_2 layer. Etching was done in three steps of 30 s after which the bottom Ti/Au electrode was exposed. Conductivity tests were performed to confirm all oxide had been removed. Surface profile measurements were also carried out to measure the etch depth thereby confirming the thickness of the etched oxide. Finally, wafers were dipped in acetone to remove all the resist, then rinse-dried ready for the next process steps (Figure 9).

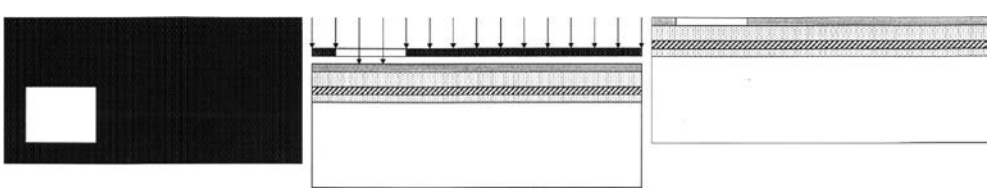
The depth of the etched SiO_2 was measured using the Detach 6M surface profilometer. The profilometer used vertical movements of the stylus along the wafer to gather topography information about the measurement. It has a vertical range from 50 Å to 262 μm with the vertical resolutions of: ± 1, 10, and 40 Å for 6.5, 65.5, and 262 μm vertical range, respectively; and a scan length of 50 μm to 30 mm with a maximum resolution of 0.067 μm for a 2,000 μm scan length.

The average etch depth of the SiO_2 was 0.5 ± 0.01 μm. Because the measured depth is greater than the thickness of the deposited SiO_2 insulating layer of 0.5 μm, it implies that all of the oxide was removed during the etching. This confirmation step is very important especially during testing because any un-wanted oxide residue would hinder access to the bottom electrode and produce weak wire bonds.

Deposition and patterning of the sacrificial layer

During this step, the sacrificial layer made of a 6 μm thick photoresist was spin-coated on the wafer, baked at 150°C, and patterned with mask M2. The thickness of this sacrificial layer sets the electrostatic gap to 2.2 μm after developing the photoresist. In this process, photoresist was used as the sacrificial layer. This is because it can be easily removed using an oxygen plasma process. Like in all previous photolithography steps, an HMDS resist adhesion promoter was vaporized on the wafer (Ronghua, 2010), followed by resist spin coating. The S1813 recipe was used to deposit 2 μm of photoresist. Wafers are then soft baked at 90°C for three minutes to dehydrate the resist and then aligned with mask M2. Contact ultra-violet (UV) exposure was then done using the 3 μm recipe for 20 s. Wafers were then developed using a 3 μm recipe. With the help of a surface profiler, the height of the spin-coated resist film was measured to confirm the sacrificial gap which determines the electrostatic gap between the cantilever and the substrate.

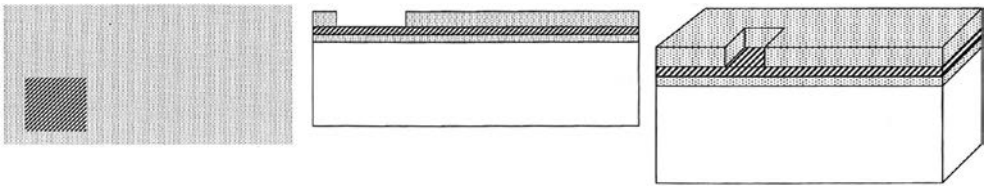
Figure 8 Patterning to expose bottom electrode using photomask M1 (dark field) and positive photoresist



(a) **(b)** **(c)**

Notes: (a) Top photomask view; (b) UV exposure side view; (c) side view after developing the resist

Figure 9 Wet etching PECVD SiO_2 using buffered HF



(a) **(b)** **(c)**

Notes: (a) Top view; (b) side view; (c) 3-D view

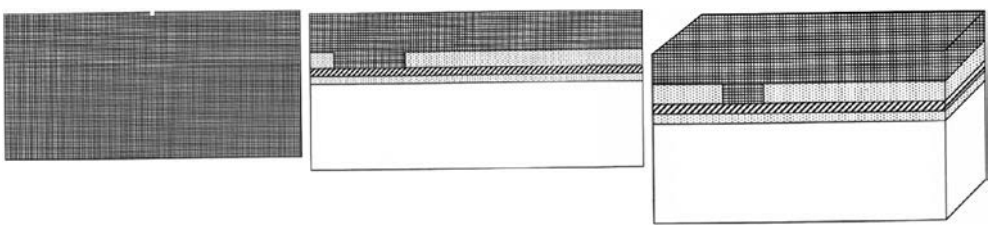
The gap between the beam and the bottom insulating oxide determines the tuning frequency range, and is one of the optimal design parameters. It is determined from the thickness of the spin-coated photoresist using the Dektak 6M surface profilometer. Measurements taken at different locations of the wafers from which an average electrostatic gap was recorded as $2.20 \pm 0.02\ \mu$m. The sketches for the spin coating of photoresist are shown in Figure 10, which were followed by UV exposure shown in Figure 11, and photoresist wet stripping to remove regions affected by the radiation, as shown in Figure 12.

Blanket deposition of Ti and Au seed layer

Titanium (Ti) metal 30 nm thick was evaporated onto the insulating first oxide. Ti readily adhered to the surface of the oxide and to the 100 nm gold seed layer.

The Ti/Au seed layer was deposited by vacuum evaporation, as a blanket deposition that covered the whole wafer comprising of the cantilever-patterned photoresist. This is important in enabling the electroplating current to reach all devices on the wafer, and is shown in the sketches in Figure 13.

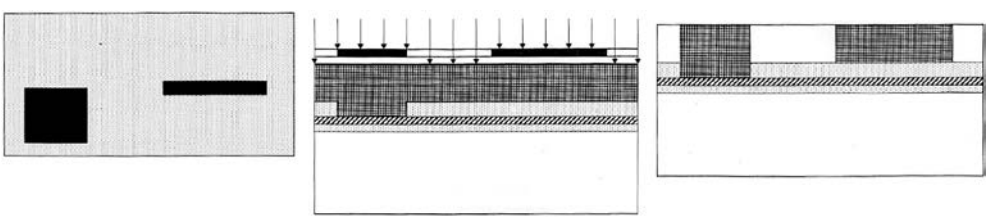
Figure 10 Positive photoresist spin coating of 7 μm maximum thickness



(a) **(b)** **(c)**

Notes: (a) Top view; (b) side view; (c) 3-D view

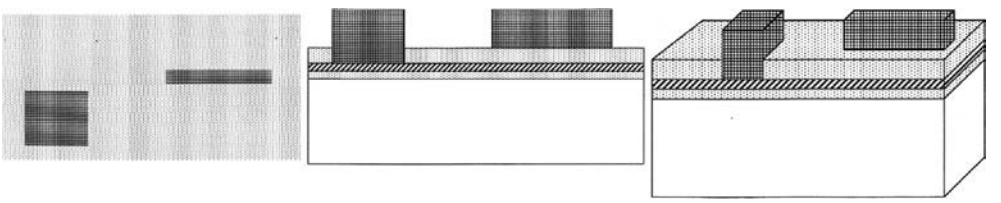
Figure 11 Patterning sacrificial layer using clear field photomask M2



(a) **(b)** **(c)**

Notes: (a) Top photomask view; (b) UV exposure side view; (c) side view after developing the resist

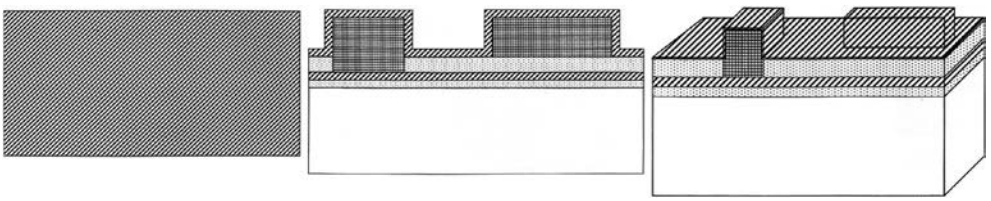
Figure 12 Photoresist strip



(a) **(b)** **(c)**

Notes: (a) Top view; (b) side view; (c) 3-D view

Figure 13 Ti/Au seed layer deposition



(a) **(b)** **(c)**

Notes: (a) Top view; (b) side view; (c) 3-D view

Photolithography defining the cantilever beams

The final patterning was done using mask M3 to define the cantilever regions and to avoid electroplated gold from reaching all other parts of the wafer. Details of the process step are shown in the sketches in Figure 14, and included photoresist spin coating, exposure with ultraviolet light, as well as developing and stripping off the resist. In the end only regions were the cantilever would be defined were left exposed ready for electroplating.

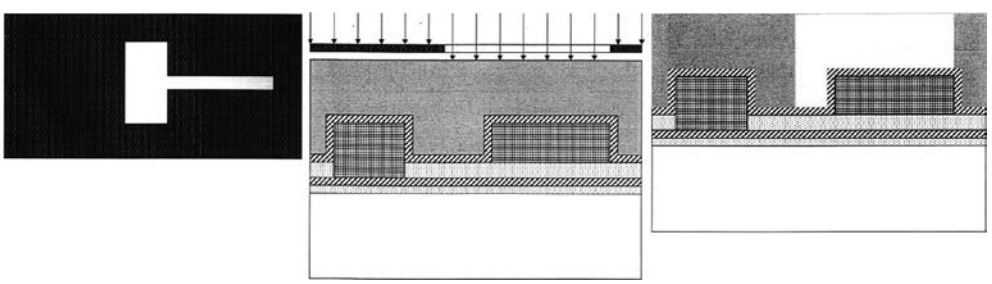
Electroplating process employed to deposit Au

In this work, the electroplating was used to deposit Au thickness of 2 μm in a thiosulfate-sulfite bath and process started with the calculation of the plating area. Sketches of the structure after electroplating are shown in Figure 15, and those after photoresist was completely removed, in Figure 16. This key parameter dictates the final thickness of the plated material (Schlesinger, 2010). The exposed area for electroplating was 5.6 cm^2. Using the atomic mass of Au of 196.67 g/mole, and a density of 19.3 g cm^{-3}, an area of 5.6 cm^2 with a plating current of 11 mA, would take approximately 20 minutes to deposit 2 μm of Au.

A low power oxygen plasma clean, also called a descum, was done to remove any remaining resist residues on the wafer that might be covering the area to be plated. The wafers were then weighed, rinsed and dried ready for plating. The plating system, based on a thiosulfate-sulfite bath, consisted of the following components: vertically mounted Perspex (polymethyl methacrylate) flow channel, a polypropylene plating reservoir equipped with a poly (tetrafluoroethylene) encased heater, a magnetically coupled pump, and a filter chamber. The various components were connected using polypropylene piping and the flow was controlled via a network of pneumatically controlled valves. A flow rate of 175 ml/s was used, and this corresponded to a turbulent flow regime.

The solution was continuously filtered through a pair of 1 μm retention polypropylene filters to remove particulates. The electrodeposition experiments were performed under constant current conditions using a computer-controlled direct current power supply (Zareian-Jahromi and Agah, 2009).

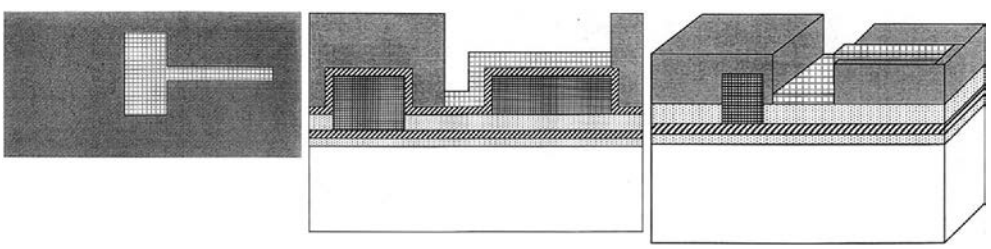
Figure 14 Thick photoresist spin-coating and UV exposure using dark field photomask M3



(a) **(b)** **(c)**

Notes: (a) Top photomask view; (b) UV exposure side view; (c) side view after developing the resist

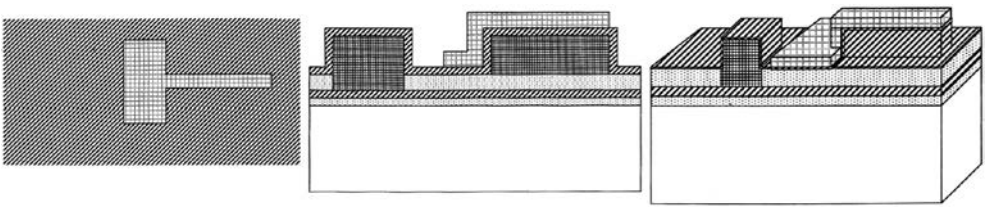
Figure 15 Au electroplating to a thickness of 2 μm on exposed parts of the seed layer deposition



(a) **(b)** **(c)**

Notes: (a) Top view; (b) side view; (c) 3-D view

Figure 16 Photoresist strip exposing electroplated Au and Ti/Au seed layer



(a) **(b)** **(c)**

Notes: (a) Top view; (b) side view; (c) 3-D view

The flow rate was measured using an in-line paddle rotameter, and the temperature in the flow channel was measured via a calibrated thermocouple. Wafers were plated in a vertical flow channel.

In the implementation of this step, the wafer was mounted on one wall of the channel and a 100 mm wide Au plate-mesh anode mounted on the opposite wall. The anode dissolved under the influence of the plating current; forming gold ions that replace those discharged thus depositing as metallic gold on the wafer which acts as the cathode. The gap between the anode and wafer cathode was 1 cm, and the width of the channel was 12 cm. The wafer sat flush with the channel wall, and the electrical contact was made via four insulated probes which contacted the front side of the wafer near the periphery.

The electroplating solution used was a ready-to-use gold electroplating solution ECF60 (sulphide gold) with a concentration of 10 g/l, and a pH of 9.4. It was allowed to circulate for 3 min prior to plating so as to allow sufficient time for thermal equilibration and to dislodge any air bubbles that may be trapped in the resist pattern. After this time, a current corresponding to the desired deposition rate was applied. A current density of 1.96 mA/cm^2 was used in the deposition. To ensure that the plating bath is homogeneously at 50°C, a magnetic stirrer was used. This helped in achieving good uniformity and delivering reactants from the bulk solution to the regions near the cathode. Other parameters used in the electroplating process included a plating voltage of 0.97 V, current of 11 mA, a flow rate of 170 ML/s, and a plating time of 20 s. These parameters were varied for different runs aimed at achieving an approximate thickness of 2 μm.

After plating, the wafers were rinsed, dried and then weighed. The patterning photoresist was then removed with a commercial resist stripper (acetone), and the Au deposited measured. The average weight of the deposited gold was measured as 29.47 ± 4.43 μm while the average gold thickness before and after removal of the Ti/Au seed layer was 2.10 ± 0.05 μm and 2.04 ± 0.05 μm, respectively. From these measurements, it is clear that the final etch of the seed layer does remove part of the beam material. Although it is important that the entire seed layer is etched away, care has to be taken to avoid reducing the beam thickness significantly. The surface roughness (measured using a surface profilometer) of the plated gold was 125 Å, which compares well with previous values of 200-250 nm (Green *et al.*, 2003). Surface roughness plays no particular importance in this work, but flat surfaces improve the reflection of the laser beams from a laser Doppler vibrometer during frequency tuning testing of the device.

Etching

Isotropic wet etching was used etching the Ti/Au seed layer. For the Au seed layer, the etchant consisted of 4 kg of Potassium Iodide (KI), 1 g of Iodine (I_2), and 40 ml of H_2O, with an etch rate of 0.5-1 μm/min (Eidelloth, 1991). For the Ti adhesion layer, the etchant used was HF:H_2O_2 with an etch rate of 880 nm/min. Au was etched with a gold etching solution by dipping water into the beaker containing the solution. Complete Au removal took 12 s, while that for Ti took 20 s.

Complete removal of the Ti/Au seed layer was confirmed by taking a resistance/conductivity measurement using a digital multimeter to probe different locations on the wafer. The large resistance measured confirmed that the whole conductive Ti/Au layer has been removed leaving the insulating SiO_2. After the wet etching of the Ti/Au seed layer, the electroplated Au structures were left on the wafer. The wafer was then rinsed in deionized water and dried. In Figure 17, the structures are sketched with the entire seed layer removed from the wafer.

Dicing

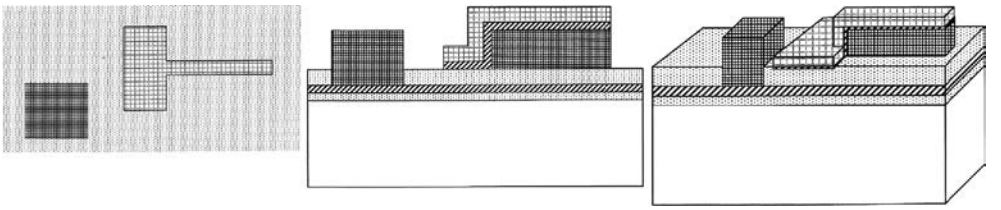
In this work, dicing was done using the Loadpoint Micro Ace Series 3 dicing saw machine (Shi *et al.*, 2009). Before the dicing, the wafer surface was coated with a layer of photoresist to protect the devices from the damage and contamination of the debris generated during the dicing process. This is because the dicing process is an aggressive one involving high pressure jets of water cooling the dicing saw. The dicing saw was programmed to automatically cut within the dicing crosses on the wafer that had been created during the photolithography steps as patterns copied transferred from the photomasks M1, M2 and M3. A picture of one of the devices diced from the wafer is shown in Figure 18.

Dry release

The electroplated gold beam structures were released by completely etching away the photoresist sacrificial layer in an oxygen (O_2) plasma asher using end-point detection and over etch technique (Bartek and Wolffenbuttel, 1998). The sketches of this step are shown in Figure 19. During the process, the flow rate of O_2 was set at 800 ml/min, the chamber pressure at $\sim$1 mbar, and the microwave power at 500 W.

To avoid carbonizing the photo-resist, the chamber temperature was set not to exceed 150°C since continuous heating of the devices may cause a higher rise in average temperature (Chatzandroulis *et al.*, 2002). Due to the different thermal expansion coefficients between the metallic films, unwanted differential stress may result and cause

Figure 17 Etching of Ti/Au seed layer



(a) **(b)** **(c)**

Notes: (a) Top view; (b) side view; (c) 3-D view

Figure 18 A diced wafer with outer markings of the sacrificial layer clearly showing around the beams and on the bottom electrode

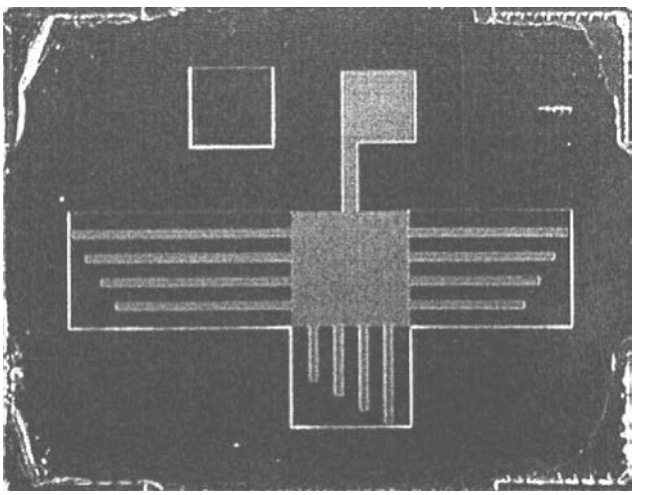
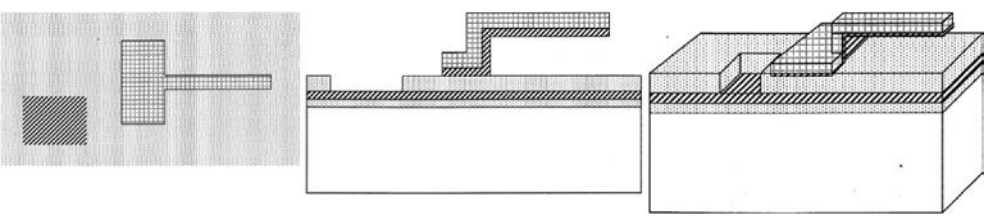


Figure 19 Oxygen plasma ashing of regions covered by photoresist to release the cantilever

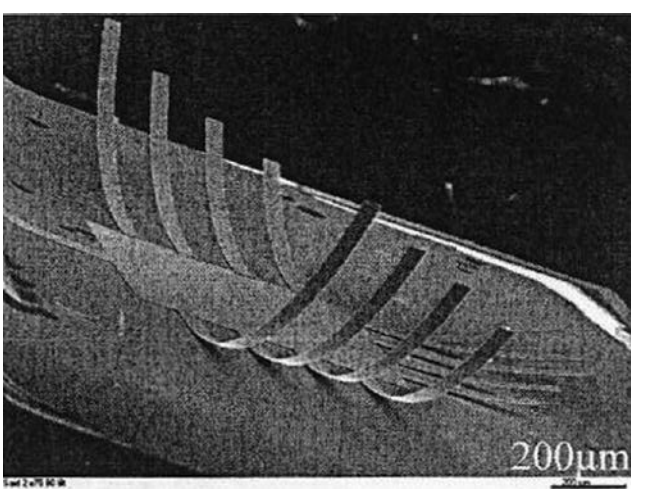


(a) **(b)** **(c)**

Notes: (a) Top view; (b) side view; (c) 3-D view

irreversible deformation. This is especially true if the strain incurred goes beyond the elastic limit of the metallic film well into the plastic regime. The ashing time was controlled to avoid inducing thermal stresses that will deform the beam after release (Mastrangelo, 1993). Ashing was carried out for 6.5 min using a 500 W plasma and for 12 min using a 250 W plasma. Figure 20 shows released cantilevers.

Figure 20 Released cantilever beams after oxygen ashing



Wire bonding

Wire bonding is a process of creating a conduction path by passing a thin metallic wire between two electrodes also called pads, or between the electrodes on the device to the chip package used for electrical testing (Qin *et al.*, 2011). In this work, a thin wire originating from a gold ball was used to connect both the top and bottom electrodes on the device to the pins on the chip package. This was done using the Kulicke and Sofa model 4124/8 Thermosonic Gold Ball Bonder. Because both electrodes are made of gold, it was easy to

attach the gold ball during the bonding. Prior to wire bonding, the device was glued to the package using UHU plus End fest 300 Epoxy-based adhesive (Harman, 1997).

Lithographic photosmasks used in this work

In this fabrication process, three photomasks (M1, M2, and M3) were used. A photomask is either a nearly optically flat low-expansion glass that is transparent to near ultraviolet (UV) or a quartz (fused silica) plate transparent to deep UV. It has 800 Å thick chromium layer patterned using e-beam lithography, which is opaque to UV light. During the UV exposure step of the photolithographic process, photomasks are placed in direct contact with photoresist-coated wafer surfaces so that a light field or dark field 1:1 image of the whole mask is transferred to the wafer surface. Contact exposure reduces mask lifetime through degradation and wear.

The masks M1, M2, and M3 were designed on a wafer template using a layout and verification editing software as three different layers 09, 10, and 11, respectively, together with the alignment and test marks for each mask. M1 was designed with a polarity of dark field using layer-09 to define the bottom electrode as well as crosses for dicing of the wafer. M2 was designed using layer-10 and manufactured with a transparent or light field and the drawn structures were in chrome (dark). It was used to define the sacrificial gap. M3 was designed using layer-11, and manufactured as a dark field mask. The mask was used to define the cantilever beam arrays and their connection to the anchor point as well as the top actuating electrode.

Patterns defined on a dark field mask will be visible on the wafer after photolithography. UV light passes through the regions left clear thus exposing the positive photoresist on the wafer. As a result the exposed resist will be removed so that the regions unprotected by the resist mask are etched away. The opposite is true for a light field mask. All masks, alignment and test mars are shown in Figure 21, while the full wafer template is shown in Figure 22.

Results and discussion

The XL30 ESEM-FEG scanning electron microscope (SEM) was used to closely inspect the released devices, to measure the cantilever thickness as well as the separation gap between the cantilever and the insulated substrate with a resolution of 2 nm (Griffin, 1994). This was done progressively as the release process was being optimized to obtain relatively flat cantilever beams. Initially, released beams were bent upwards due to residual stress as shown in Figure 23. These devices were released with a plasma power of 500 W after 12 min of oxygen ashing.

After lowering the oxygen plasma power to 250 W, and the ashing release time to 7.5 min, flat beams were observed as shown in Figure 24. To analyse the gap between the beams and the substrate, close-up views of the beam tips and sides were taken as shown in Figure 25. Additionally, the thickness of the beam was measured as shown in Figure 26.

The Olympus MX 50T inspection microscope attached to a BRSL "David" measurement system was used for visual inspection of the manufactured devices at various process steps for defects and to measure the dimensions with 0.5 μm accuracy (Newboe, 1991). The overall dimensions of the device are as shown in Table I. Line and width dimensional measurements of the shorter cantilever are shown in Figure 27.

From the results shown in the preceding paragraphs, it is evident that initially, the released beams were not ideally flat. The end-tip was bent upwards with the initial deflection increasing with the length of the beam as shown in Figure 23. This bending was attributed to several factors: first the high temperatures that are involved in the oxygen ashing process introduced thermal stresses. These temperatures depended on the oxygen plasma power and the duration of the ashing process. As the device was removed from the asher, the difference in temperature causes the beam tip to bend since the other end is fixed. Second, there could have been a deposition tensile stress due to the electroplating bath. This is because several wafers based on different processes were used in the same plating bath as this work. These wafers might have introduced impurities in the plating solution that resulted in a change in the stress of the deposited Au film. Other factors that could have resulted in a change in the stress include: the bath life and aging of the plating solution; plating without additives, accelerators and suppressors in the solution that should have increased plating throwing power and uniformity; and not annealing the device after plating. Additionally, the upward bending could also be attributed to the thermal mismatch between the thin Ti metal underneath the Au seed layer, and the electroplated Au.

On the whole, the deflection of the released cantilever beams was dependent on the dry-release ashing process time, and it was concluded that thermal stress was incurred during the plasma etching process. Since this additional stress can be inconclusively distinguished from the deposition stress, the post-deposition process such as a dry-release method also needs to be controlled for accurate characterization. Several solutions might be available including the use of a bridge (fixed-fixed) beam configuration to cancel the stresses.

Figure 21 (a) Photomask M1; (b) Photomask M2; (c) M3 photomask; (d) Alignment mark for M1; (e) Alignment mark for M2; (f) Alignment mark for M3; (g) Test marks for all masks M1, M2, M3

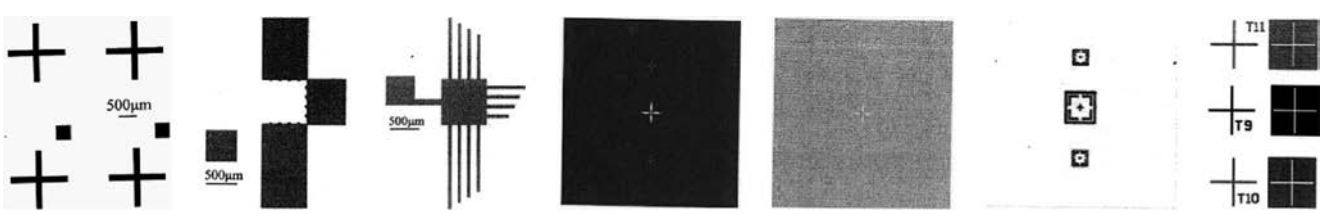


Figure 22 Full wafer template

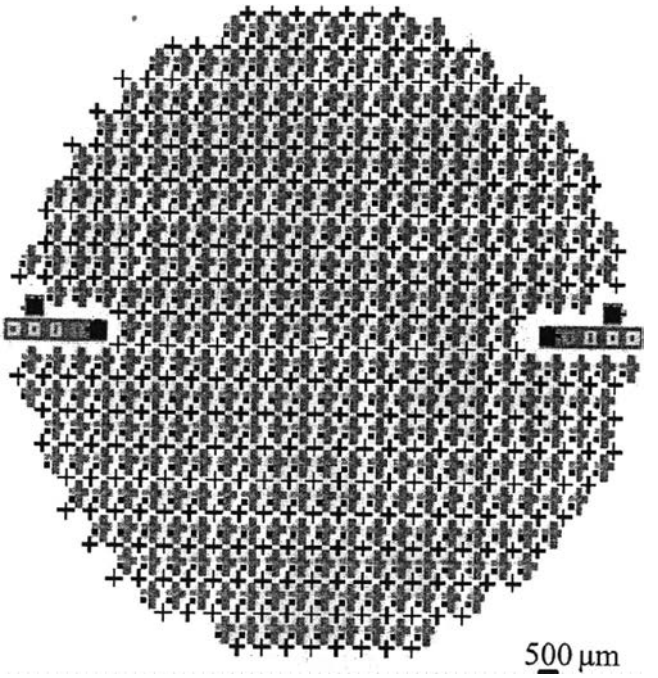
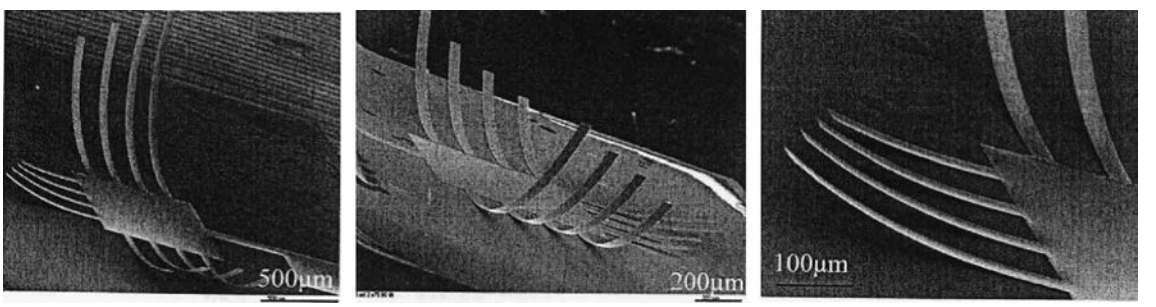


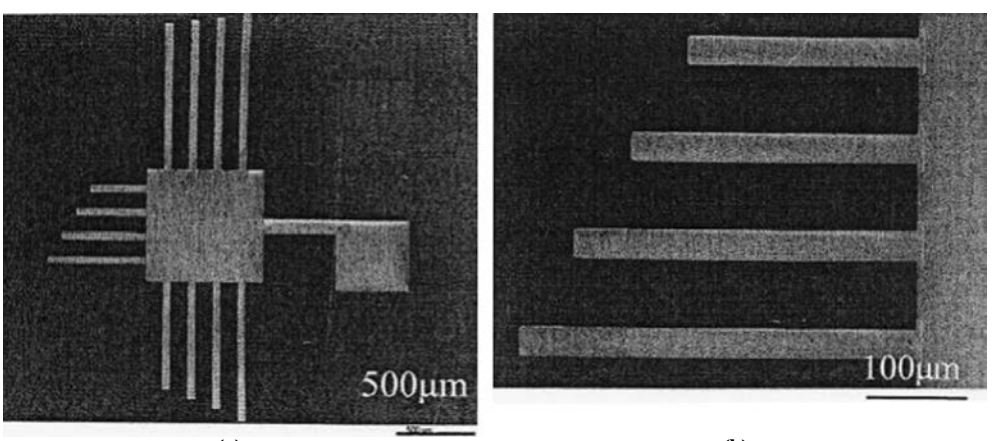
Figure 23 SEM images of the suspended beams before the oxygen plasma ashing power was optimised



(a) **(b)** **(c)**

Notes: (a) All beams wide view; (b) close up view of the longer beams; (c) close-up view of the shorter beams

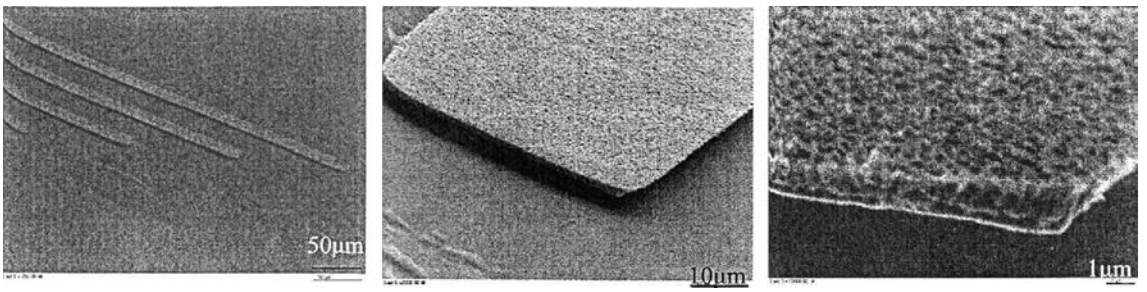
Figure 24 SEM images of the flat beams after optimising the plasma ashing process



(a) **(b)**

Notes: (a) All beams wide view; (b) close-up view of the shorter beams

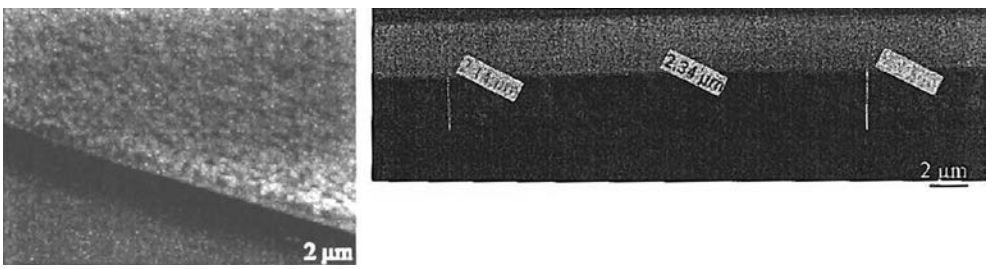
Figure 25 SEM images of the flat beams after optimising the plasma ashing process



(a) **(b)** **(c)**

Notes: (a) Some of the longer beams wide view; (b) close-up view of the beam; (c) a much closer view of the beam for thickness measurement

Figure 26 SEM images of the flat beams after optimising the plasma ashing process



(a) **(b)**

Notes: (a) Some of the longer beams wide view; (b) close-up view of the beam

Table I Results of optical measurements of the beam dimensions

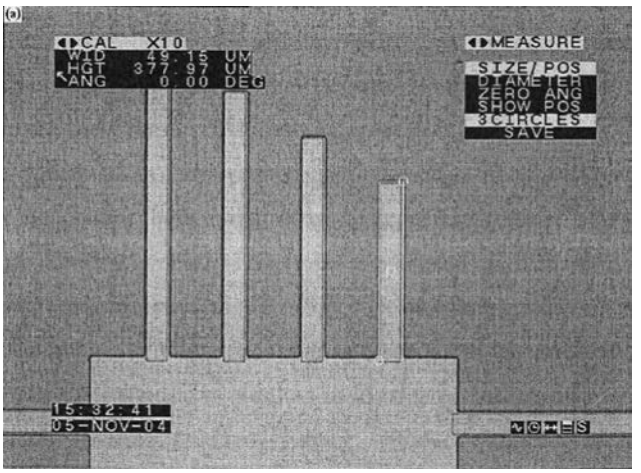
Device ID	Beam length Lo ± 0.01 (μm)	Beam width b ± 1.12 (μm)	Beam thickness d ± 0.03 (μm)	Electrostatic gap H ± 0.63 (μm)
Beam 1	377.97	49.05	2.15	2.48
Beam 2	495.50	53.66	2.24	2.31
Beam 3	598.20	51.86	2.23	2.15
Beam 4	699.10	52.86	2.18	2.42
Beam 5	800.00	55.86	2.21	2.01
Beam 6	891.00	50.25	2.23	2.49
Beam 7	992.79	52.86	2.21	2.37
Beam 8	1,090.09	49.86	2.25	2.16
Beam 9	1,192.79	53.66	2.15	2.05
Beam 10	1,290.09	50.45	2.22	2.30
Beam 11	1,390.99	51.66	2.16	2.23
Beam 12	1,491.89	52.66	2.14	2.48

An immediate solution, which was employed in this work was to change the ashing process recipe to allow for low plasma power and intermittent ashing. Results show that an optimum ashing time can be reached where the beams are almost entirely flat. These are shown in Figures 24 and 25. No stiction was observed in the cantilevers.

Conclusion (and recommendations)

A fabrication process for the length tuning device has been described. The process followed a surface micromachining procedure on a silicon wafer as a substrate. Standard lithography techniques were employed in the fabrication process and a set of three lithographic masks used to define the component layers of the cantilever device have been illustrated. The device after fabrication consisted of cantilever arrays that, together with the bottom electrode, form a vibrating microelecromechanical (MEMS) device. The fabrication recipe involved spin-coated resist as the sacrificial layer, which was dry etched using oxygen plasma ashing to release the cantilevers. The vibrating microstructure was made out of electroplated Au. By lowering the plasma power, and decreasing the ashing time, stresses induced during the release process were reduced thus avoiding stress-induced bending of the cantilever tips. The released cantilevers were relatively flat and stiction free with dimensions ranging from 377.97 ± 0.01 μm to 1,491.89 ± 0.01 μm in beam length, 52.06 ± 1.93 μm beam

Figure 27 Optical microscope dimensional measurements for the shorter beams



width, 2.21 ± 0.05 μm beam thickness, and an electrostatic gap of 2.29 ± 0.17 μm above a 4,934 ± 3 Å thick SiO_2 insulation between the two electrodes.

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