

Silicon Photonics Neuromorphic Computing and its Application to Telecommunications (invited)

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Abstract We present simulations on the brain-inspired paradigm of Photonic Reservoir Computing integrated on a silicon photonics chips as a promising alternative to solve problems like non-linear dispersion compensation in the analogue optical domain, without requiring complicated electric DSP.

Introduction

In this paper, we propose a novel signal equalizer to undo both linear and nonlinear impairments in optical communication networks based on reservoir computing and study its performance in IM-DD links. Our approach is based on the neuromorphic concept of Reservoir Computing and operates in the optical domain. This means that it is very fast, compact and energy efficient. Additionally being CMOS-compatible means that we can take advantages of CMOS mass production benefits for scaling. Moreover it can easily be co-integrated with receiver electronics via monolithic photonic-electronic co-integration in, for example, a transceiver module.

Photonic Reservoir Computing

Reservoir Computing (RC) is a brain-inspired non-Von-Neumann analog computing approach that relies on the information processing capabilities of certain physical systems^{2,4,8}. Initially invented as a software technique for processing temporal data on digital computers, reservoir computing has evolved into a computationally versatile platform capable of tackling a wide range of tasks. It excels at tackling tasks that involve sequential data and require a finite amount of memory, such as speech recognition and time series prediction. A key extension to reservoir computing is implementing the reservoir in hardware. Examples of RC implemented in mechanical systems, memristive systems, atomic switch networks, boolean logic elements and photonics as substrates can be found in^{1,3,5,6}.

The RC system consists of three basic parts: an input layer which couples the input signal into a non-linear dynamical system, "the reservoir" (i.e. the recurrent neural network, which is kept untrained) and finally the output layer that typically

linearly combines the states of the reservoir to provide the time-dependent output signal. An illustration of this architecture is given in Fig. 1.

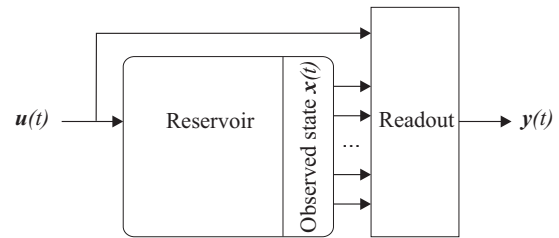


Fig. 1: Schematic representation of a reservoir computing system. The input signal $u(t)$ is fed into the reservoir and the resulting reservoir states $x(t)$ are used to learn a linear readout that is then used to generate the output signal $y(t)$.

The way to apply the RC approach to solve a particular task typically takes the form of setting it up as a supervised machine learning (linear regression) problem. Known labeled data (training examples) is used to train the weights to compute the output (the readout) that is typically a linear combination of the recorded signals at each reservoir node. These weights are then stored and used to generate the output signal for future input signal sequences. RC systems are fast to train and have shown state-of-the-art performance on time-dependent data (such as speech recognition, nonlinear channel equalization, robot control, time series prediction, financial forecasting, handwriting recognition, etc.) on a range of complex tasks.

Passive photonic reservoirs are a more recent invention in which the input signal propagates through a passive linear photonic network, i.e., one without amplification or nonlinear elements. The required nonlinearity is introduced at the readout point, typically with a photodetector^{7,9}. The photonic reservoir computing equalizer in this work is based on the passive integrated reservoir design that was introduced in⁷. Apart from sim-

plexity from a fabrication point-of-view, a further advantage of such a passive architecture is the reduced power consumption, since the computation itself does not require external energy. As in⁷, the reservoir nodes are laid out in a swirl topology to satisfy planarity constraints of the CMOS SOI platform while allowing for a reasonable mixing of the input signals.

In discretized time, the passive reservoir state update equation can be generalized as:

$$\vec{x}[k+1] = \mathbf{W}_{res}\vec{x}[k] + \vec{w}_{in}(\vec{u}[k+1] + u_{bias}) \quad (1)$$

where \vec{u} is the input to the reservoir and u_{bias} is a fixed scalar bias applied to the inputs of the reservoir. For an N -node reservoir, \mathbf{W}_{res} is an $N \times N$ matrix representing the interconnections between reservoir components taking into account splitting ratios and losses, with phases drawn from a random uniform distribution on $[-\pi, \pi]$, $U(-\pi, \pi)$. \vec{w}_{in} is an N -dimensional column vector whose elements are nonzero for each active input node. These input weights are similarly chosen from $U(-\pi, \pi)$.

Our previous work in⁷ experimentally verifies that a passive integrated photonic reservoir can yield error-free performance on the header recognition task for headers up to 3 bits in length, as well as on a number of digital optical bit level manipulations that could be useful for various telecommunications tasks such as parity, coding, etc.

Here, we present an equalizer implemented using an integrated photonics reservoir computing (PhRC) system. Conceptually, the PhRC equalizer is a high-dimensional complex nonlinear filter that acts in the optical domain to undo both linear and nonlinear distortions. The PhRC equalizer will naturally benefit from the advantages of the CMOS platform in terms of scalability and energy efficiency. The design is flexible and can be applied to virtually all sorts of links without limit in terms of required bandwidth. Designing a 40Gb/s or a 400Gb/s equalizer is a matter of changing the internal timescale of the reservoir (set by the length of the delay lines); the ultimate limit lies in the readout electronics, making the PhRC equalizer a future-proof option to signal equalization. Once deployed, the equalizer can easily be re-trained in the field (on demand or on a schedule) to adapt to the link conditions. The PhRC equalizer could also be deployed just before a DSP to reduce the computational load associated

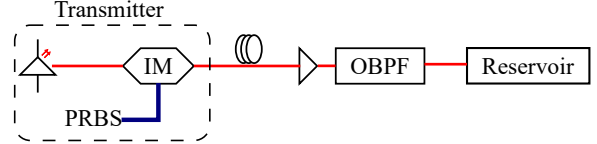


Fig. 2: Schematic representation of the simulation setup to generate data for the signal equalization task. The input pseudo-random bit sequence (PRBS) signal is modulated onto a laser signal, transmitted over a fiber link, amplified and filtered, after which the field of the optical signal is saved to file to be used as input to the photonic reservoir simulation model. OBPF - Optical band pass filter.

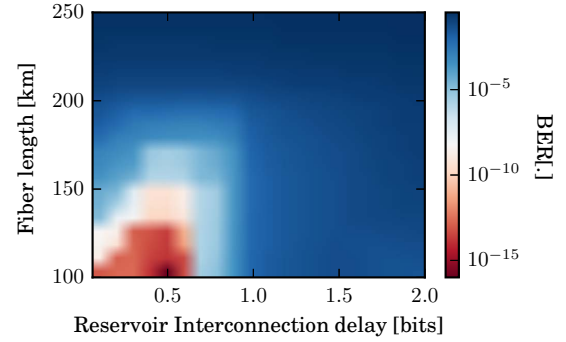


Fig. 3: Error rates vs reservoir interconnection delay and fiber length for 16 node PhRC equalizer for an NRZ-OOK link at 10Gb/s.

with cleaning up severely distorted signals. We will show numerical simulations of the equalizer operating under various conditions for realistic fibre optical links using the resulting Bit Error Rate as the performance metric.

Equalisation of Metro Links

In this section, we investigate the performance of the PhRC equalizer on unrepeated fiber optic communications links in the metro regime for fiber lengths ranging from 100km to 250km for a 10Gb/s NRZ OOK link. The setup is shown as in Figure 2. The amplifier is set to entirely undo the link attenuation and the filter gets rid of out-of-band noise and is a 3rd order Bessel filter with bandwidth 4 times the data rate. Note that this data rate is chosen here to keep it compatible with the measurement capability in our characterization lab but the same procedure can be followed for higher speed links.

First, we study the influence of the node interconnection delay time on the BER of the PhRC equalizer. The node interconnection delay is the most important parameter for passive planar integrated photonics reservoirs as it determines the timescale at which signals interfere within the reservoir. It is set by changing the length on the on-chip delay lines at design time.

As seen in Figure 3, the regime of best operation of the PhRC equalizer corresponds to an interconnection length that corresponds to a de-

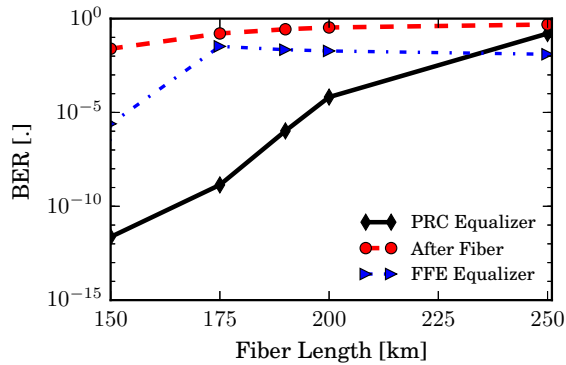


Fig. 4: BER of the PhRC equalizer as compared to that of an FIR Feed Forward Equalizer (FFE) trained on the same amount of data for different fiber lengths. The launch power is set to 15 mW.

lay of half the bit duration. This result demonstrates that under these link conditions, the condition of the optimal interconnection delay coincides with those for the header recognition and bit level tasks of⁷. For the rest of the discussions in this section we therefore fix the interconnection length of the reservoir to this value.

As in any causal system, the reservoir output requires a finite time before responding to the input. We therefore need to find the delay between the input and the corresponding desired output for which the reservoir can best solve the task. This delay is termed latency in this work (we assume here that there are no external, more rigid latency constraints to take into account). In the interconnection delay studies above (as illustrated in Figure 3), we arbitrarily set the value of the latency to 1 bit duration. Further simulations show that the latency has a significant impact on the performance of the reservoir. The best latency corresponds to a delay of about 1 bit duration and yields almost 20dB better BER values than the case where the latency of the PhRC is ignored.

For all remaining simulations, we therefore set the reservoir inter-node delay time to half the data rate and the latency to 1 bit duration. Finally, we compare the performance of the PhRC equalizer for a link with a launch power of 15 mW - at which nonlinearities in the fiber are significant - to an FIR FFE filter trained on the same amount of data. The results are shown in Figure 4. The PhRC equalizer outperforms the FFE equalizer with BERs over 5 orders of magnitude lower at, for example, 150km and an order or two of magnitude lower at 200km. The difference in performance is a demonstration that the PhRC equalizer is a nonlinear compensation device.

Conclusion

In this paper, we have presented a design for an integrated photonics reservoir equalizer that can undo linear and nonlinear imperfections in optical communication links. We have numerically studied the performance of this PhRC equalizer for metro links. We can reach below the SD-FEC limit for links up to 200 km. In the future, we expect this task will serve as an important experimental benchmark for our integrated photonics reservoirs targeted at optical communication tasks.

Acknowledgements

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